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EXAMINER	
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ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/706,657	STULTZ, PAUL D.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6-8 and 10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6-8 and 10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 4 and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Murty et al. (US Publication Number 2003/0046464, hereinafter "Murty").

3. As per claim 1, Murty teaches an information handling system (element 100, figure 1), comprising: a plurality of processors (logical processors, elements 120(1)-120(n), figure 1) coupled to a processor bus (channel, element 180, figure 1, bus, element 254, figure 2); and a memory (memory, element 160, figure 1); wherein a processor of the plurality of processors is assigned to perform processing tasks associated with an interrupt (paragraph [0026]), wherein each of the processors is operable to enter an interrupt mode (interrupt handler, element 170, figure 1) and be serially released from the interrupt mode so as to reduce contention by the processors for system resources upon release from the interrupt mode (exit the interrupt-handler, paragraphs [0027 and 0049]), and wherein the processors are operable to be serially released form the interrupt mode according to a predetermined time delay following the release of each successive processor from the interrupt mode (releasing from interrupt mode at a time, paragraph [0046]), and wherein the processor assigned to perform the

processing tasks associated the interrupt is operable to initiate the release of every other processor from interrupt mode on a timed release (time for resetting and release, paragraph [0046]) basis following the completion by the assigned processor of the processing tasks associated with the interrupt (flags dictate release of processors, paragraphs [0044-0045]).

The Examiner notes that the processors of Murty are "operable "to be serially released and "operable" to initiate the release and no teachings of Murty preclude operability and do not stipulate that the "operable" steps of the claim limitations cannot be accomplished by the prior art.

Furthermore, in order to assist the applicant to better understand the rejection of the claim limitation "serially released" the Examiner points to paragraph 0027. The system of Murty consists of multiple processors arranged from 120(1) to 120(n) each associated with a thread. Consequently the order of operation for tasks handled by all the processors will also occur in the same 1 to n order. In paragraph 0027 and 0049 Murty teaches that each logical processor from 1 to n will execute a first code segment in consecutive order, which will bring it into the interrupt mode. During the interrupt-handling mode the first processor will initiate a flag as seen in paragraph 0034 and handle the interrupt and exit. The next processors will serially execute the first code segment and check the flag for interrupt handling and serially will be released in consecutive order 1 to n, by the interrupt handler as seen in paragraph 0027 and 0049.

4. As per claim 4, Murty teaches an information handling system of claim 1, wherein the serial release from the interrupt mode reduces contention by the processors for control of the processor bus and memory (in a series after the first processor to handles the interrupt, releasing each following processor to resume its pre-interruption activities, paragraph [0042]).

5. As per claim 6, Murty teaches an information handling system of claim 5, wherein the processor assigned to perform the processing tasks associated with the interrupt is operable to exit from interrupt mode following the release of every other processor from interrupt mode (first logical processor acts as interrupt handler and following release of other processors and execution of the interrupt-handler the first logical processor releases, paragraph [0049]).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murty in view of Carmean et al. (US Patent Number 5,809,314, hereinafter "Carmean").

8. As per claim 3, Murty fails to explicitly teach an information handling system wherein the interrupt mode is system management interrupt mode.

Carmean teaches a method for exiting from an interrupt mode in a multiple processor system of claim 14, wherein the interrupt mode is system management interrupt mode (column 3, lines 31 – 47).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify Murty with the above teachings of Carmean. One of ordinary skill would have been motivated to make such modification in order to implement power management functionality to a multiprocessor system (column 3, lines 31 – 47).

9. Claims 7, 8, 10 – 15, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murty in view of Giles (US Patent Number 6,857,084).

10. As per claims 7 and 17, Murty teaches a method for exiting from an interrupt in a multiple processor computer system (element 100, figure 1), wherein each of the processors (logical processors, element 120, figure 1) are coupled to a processor bus (channel, element 180, figure 1, bus, element 254, figure 2), comprising the steps of: for each processor, setting an indicator associated with the respective processor (the indicator is the flag which comprises multiple bits, one bit associated with each processor to express its interrupt handling characteristics, paragraph [0044], processor

access its corresponding bit) to indicate that the processor is in an interrupt mode (flag, paragraph [0034]); identifying the interrupt handling processor responsible for performing the processing tasks necessary to resolve the interrupt condition (first logical processor reads first value in ICR, paragraph [0033]); identifying the non-interrupt handling processors not responsible for performing the processing tasks necessary to resolve the interrupt condition (for each further logical processor reads a second value in ICR and is deemed as non-interrupt processor, paragraph [0033]); for the interrupt handling processor, performing the processing tasks necessary to resolve the interrupt condition; and for the interrupt handling processor, following the completion of the processing tasks necessary for resolving the interrupt, initiating the serial exit of the non-interrupt handling processors from interrupt mode, whereby contention by the non-interrupt handling processors for control of the processor bus is reduced (executes a first segment code to enter the interrupt handler, paragraph [0041], thereafter each processor accesses an indicator flag to express its interrupt handling characteristics, paragraph [0043-0044]).

Murty fails to teach a method for exiting form an interrupt in a multiple processor computer system wherein for each non-interrupt handling processor, determining whether each non-interrupt handling processor was in a halt state immediately before entering the interrupt mode; for each non-interrupt handling processor, remaining in an interrupt mode until initiated to exit the interrupt mode by the interrupt handling processor.

Giles analogously teaches a method for exiting from an interrupt in a multiple processor computer system wherein for each non-interrupt handling processor, determining whether each non-interrupt handling processor was in a halt state immediately before entering the interrupt mode (processors are halted as entering the debug mode, column 2, lines 40 – 49); for each non-interrupt handling processor, remaining in an interrupt mode until initiated to exit the interrupt mode by the interrupt handling processor (halting other processors while the interrupt is handled, column 2, lines 1 – 23).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the teachings or Murty with the teachings of Giles. One of ordinary skill would have been motivated to make such modification in order to greatly simplify the task of debugging and interrupt handling in a multiprocessor system (column 2, lines 21 – 23).

11. As per claims 8 and 19, Murty teaches a method for exiting from an interrupt mode in a multiple processor system comprising step of: for the interrupt handling processor, exiting from interrupt mode after each of the non-interrupt handling processors have exited from interrupt mode (non-interrupt handling processors return from the interrupt handler once the interrupt has been claimed and the interrupt handling processor exits therefore after the interrupt has been handled, paragraph [0049]).

12. Murty modified by the teachings of Giles as applied above in claim 7, as per claims 10 and 20, teaches a method for exiting from an interrupt mode in a multiple processor system wherein the step of remaining in an interrupt mode until initiated to exit the interrupt mode by the interrupt handling processor comprises the step of remaining in an interrupt mode until the interrupt handling processor resets (debug reset signal element 32, figure 1) an indicator as an instruction to the non-interrupt handling processor to exit from the interrupt mode (non-interrupt processors, 12a, 12b and 12c are brought out of the interrupt before the interrupt handling processor, column 8, lines 46 – 64).

13. Murty modified by the teachings of Giles as applied above in claim 7, as per claim 11, teaches a method for exiting from an interrupt mode in a multiple processor system comprising the step of, for each non-interrupt handling processor, identifying whether the processor was in a halt state immediately before entering an interrupt mode (state and conditions maintained for examination and evaluation, column 4, lines 39 – 56).

14. As per claim 12, Murty teaches a method for exiting from an interrupt mode in a multiple processor system comprising the step of causing to exit from interrupt mode those non-interrupt handling processors identified as being in a halt state immediately before entering an interrupt mode, without respect to whether the indicator has been

reset by the interrupt handling processor (all processors entering the interrupt mode including those with prior halt state that are non-interrupt read a second value in ICR and return to the previous state without regard to any reset, paragraph [0033]).

15. As per claim 13, Murty teaches a method for exiting from an interrupt mode in a multiple processor system of claim 10, wherein the indicator for a respective processor is a bit stored in a memory space associated the respective processor (memory stores interrupt handling instructions, paragraph [0022]).

16. Murty modified by the teachings of Giles as applied above in claim 7, as per claim 14, teaches a method for exiting from an interrupt mode in a multiple processor system of claim 13, wherein the step of initiating on a serial basis the exit of each non-interrupt handling processor from interrupt mode comprises the steps of: resetting a bit associated with a first non-interrupt handling processor (column 8, lines 16 – 29); pausing for a time period (propagation and transition delay, column 8, lines 18 – 21) ; and repeating the steps of resetting and pausing until the interrupt handling processor has initiated the exit of each non-interrupt handling processor from interrupt mode (the debug event de-asserts the debug event signal in bringing out the non-interrupt handling processors, column 8, lines 30 – 44).

17. Murty modified by the teachings of Giles as applied above in claim 7, as per claim 15, teaches a method for exiting from an interrupt mode in a multiple processor

system of claim 14, wherein the time period is a predetermined time period associated with a time sufficient to permit a processor to exit from an interrupt mode without contention for a processor bus or memory in the computer system (sufficient period of time during which the debug event de-asserts the debug event, column 8, lines 30 – 64).

18. Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murty in view of Giles, and in further view of Carmean.

19. As per claims 16 and 18, the combination of Murty and Giles fails to explicitly teach a method for exiting from an interrupt mode in a multiple processor system wherein the interrupt mode is an interrupt mode associated with a system management interrupt.

Carmean teaches a method for exiting from an interrupt mode in a multiple processor system of claim 14, wherein the interrupt mode is an interrupt mode associated with a system management interrupt (column 3, lines 31 – 47).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Murty and Giles with the above teachings of Carmean. One of ordinary skill would have been motivated to make such modification in order to implement power management functionality to a multiprocessor system (column 3, lines 31 – 47).

Response to Arguments

20. Applicant's arguments filed 11/19/2007 have been fully considered but they are not persuasive. The applicant argues:

1.) Murty does not disclose non-interrupt handling processors being operable to be serially released from the interrupt mode according to a timed release basis.

2.) Murty does not mention serial release from the interrupt handling mode on a timed release basis and where the interrupt-handling processor is operable to initiate the release of every other processor upon the completion.

21. As per argument 1, the Examiner respectfully disagrees. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., non-interrupt handling processors time delay) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). There is no mention of **non-interrupt** handling processors in claims 1, 2, 4, 5 and 6 as argued by the Applicant.

22. As per argument 2, the Examiner respectfully disagrees. The Applicant argues that processors of Murty are not serially released and furthermore the assigned processor is not *operable* to initiate the release of every other processor. For the argument regarding the serial release the Applicant is directed to the rejection above in

which the processors in the cited embodiment are serially released based upon a predetermined intrinsic access time delay upon determining the interrupt is being handled. In regards to the argument of the assigned processor being *operable* to release the other processors from the interrupt mode, the Examiner notes that there is no teachings in Murty that preclude the *operability* of the assigned processor to "initiate" a release. The claim limitations do not necessitate the release being a directly related to assigned processor but in fact necessitate a limitation in which the assigned processor can upon complete provide an additional signal to "initiate" a release of any pre-pending processors. There is no positive recitation of a release being initiated or that other "non-assigned" processors are release by the assigned processor. Murty teaches an initiation of a release signal toggled by the assigned processor upon completion of the interrupt handling as seen in paragraphs [0042 - 0049]. Clearly from this explanation and citation one of ordinary skill in the art would recognize the operability of the assigned processor of Murty initiating a release from the interrupt mode upon completion of the processing tasks associated with the interrupt.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on (571)272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AH

2/4/08

HENRY TSAI
SUPERVISORY PATENT EXAMINER